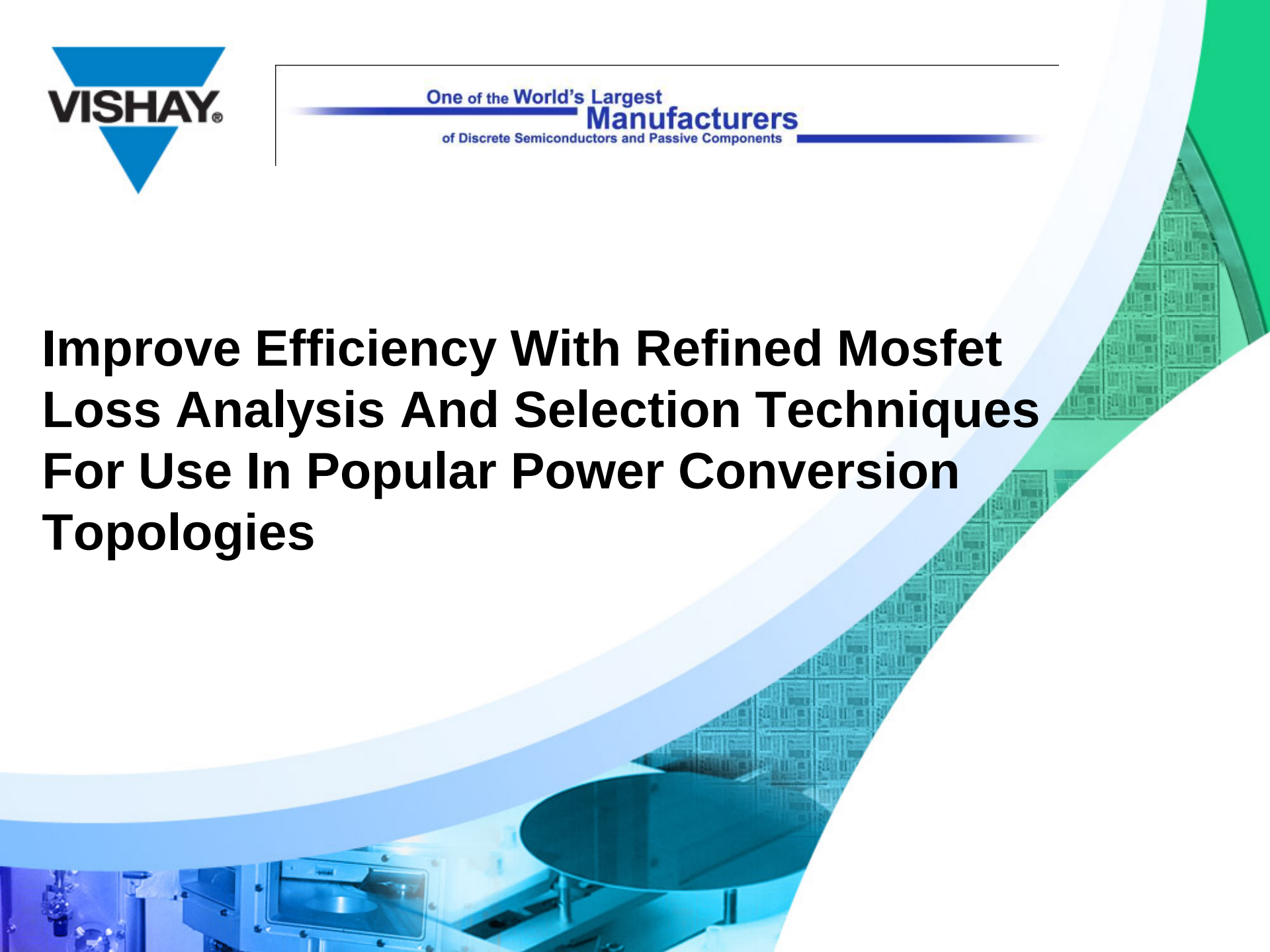
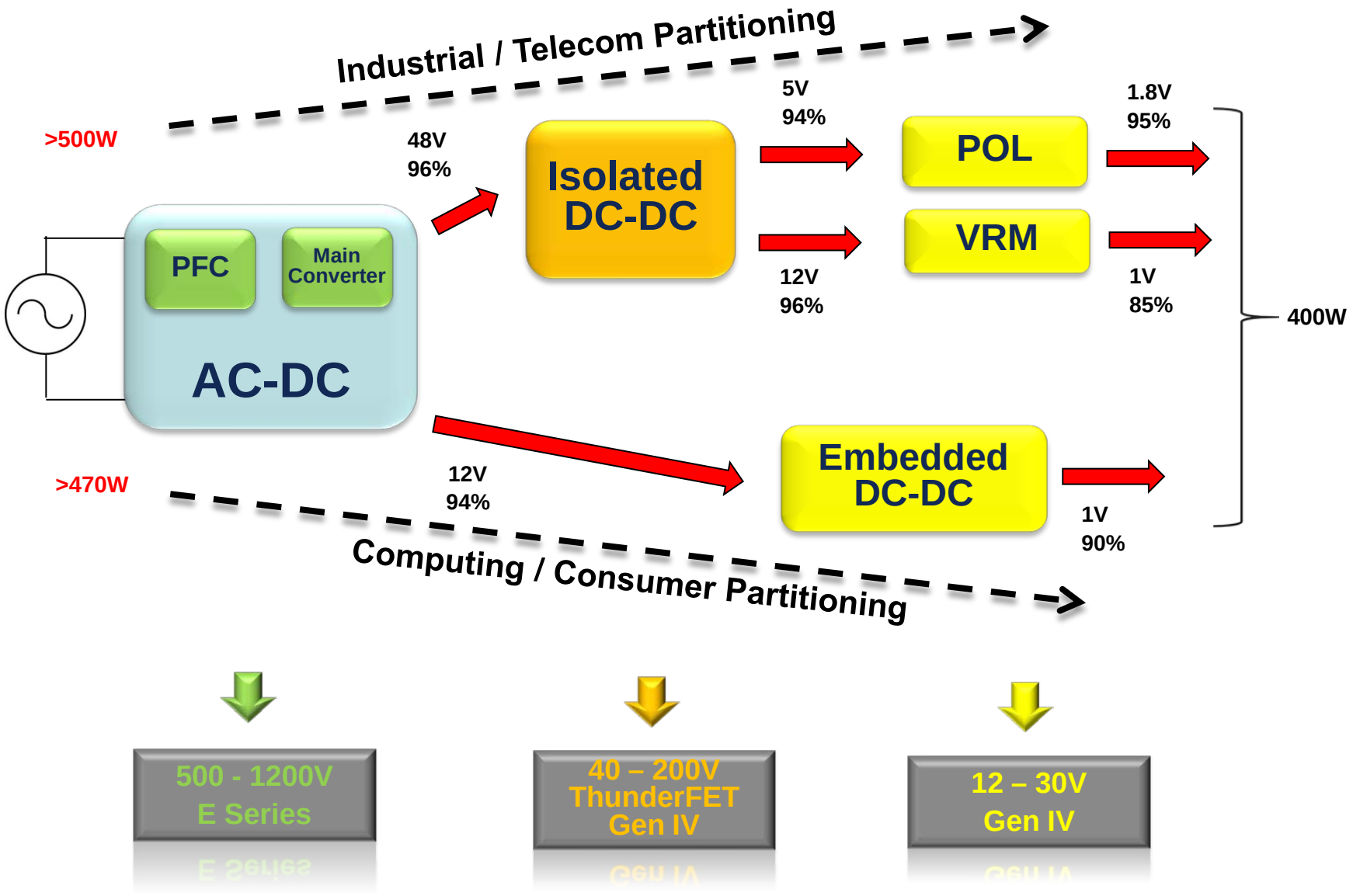
VISHAY

One of the World's Largest Manufacturers
of Discrete Semiconductors and Passive Components

Improve Efficiency With Refined Mosfet Loss Analysis And Selection Techniques For Use In Popular Power Conversion Topologies

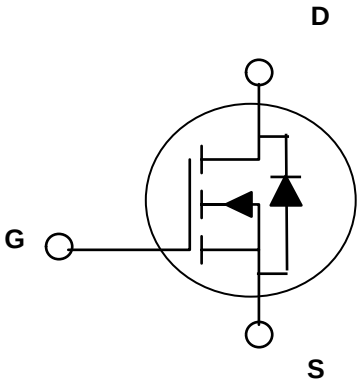


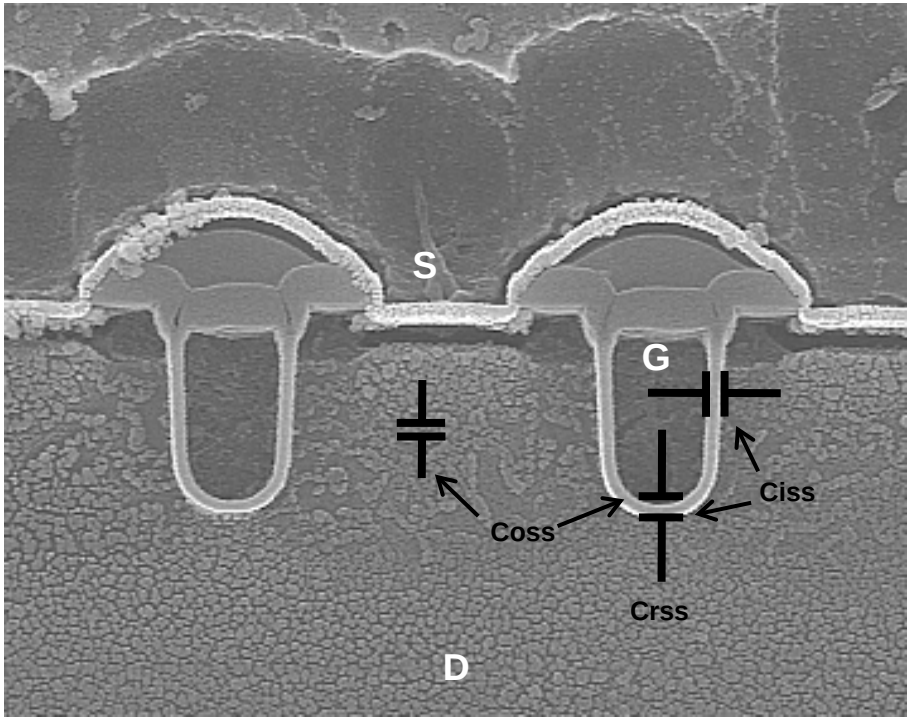
Power Conversion Building Blocks



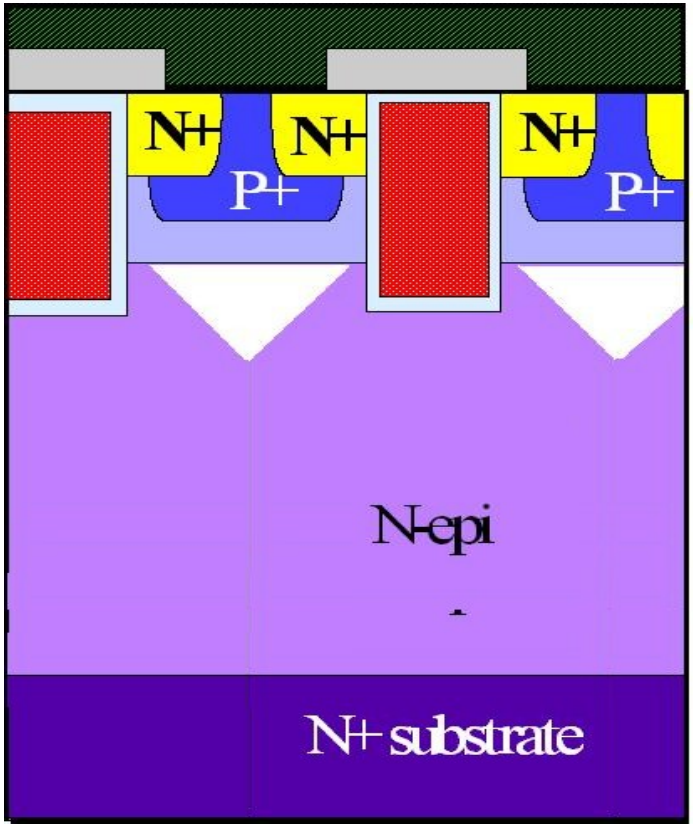
MOSFET Technology Evolution

- Achieve the lowest $R_{DS(on)}$, (RdsA) without sacrificing switching performance
  - Continue to increase cell density (more channels in parallel)
  - Shallow Junctions / Short Channels
  - Deeper Trenches / Charge balancing
  - Highly doped materials
  - Thinner wafers
  - Improved Packaging





MOSFET Components of Resistance



BVdss	30V	100V	600V
Rch:	35%	8%	3%
Repi:	35%	88%	96%
Rsub:	30%	3%	1%
Total Si	1.2mΩ	15mΩ	1.5Ω
New technologies from Vishay : Total Si	0.5mΩ	5mΩ	300mΩ

12 – 30V Gen IV

40 – 200V ThunderFET Gen IV

500 - 1200V E Series

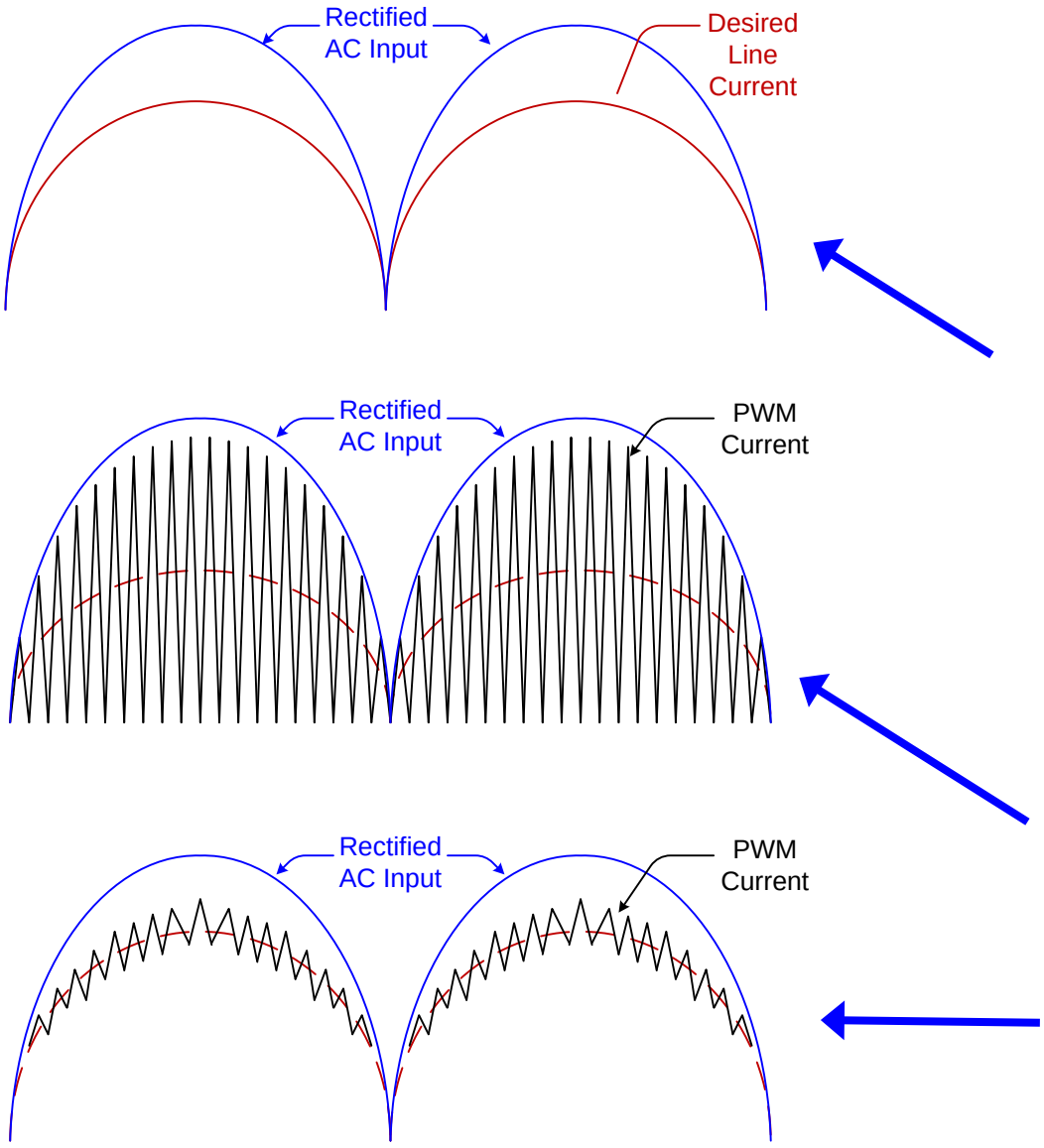
FOM Discussion

- Historically power Mosfet industry uses a Figure of Merit defined as Rdson x Qg
  - Lower the FOM better is the device
    - Can carry more current and switch faster at the same time
- Recently there is considerable rethinking on the issue
- Problem is that this definition is “blind” to the application
  - Operating conditions show over two orders of magnitude variation in frequency, voltages and currents.
- Designers choose their device based on several considerations
  - Most important being loss and efficiency
  - There is no common formula for losses

The Application Specific FOM

- Nearly a dozen “standard” topologies in use today
  - Each with its own distribution of losses
  - Conduction losses dominate LS Mosfet losses but switching losses dominate HS Mosfet in a synchronous buck
  - FOM does not account for Coss and body diode related losses
- Bottom line – we need Application Specific FOM
  - One number does not fit all!

AC-DC: Power Factor Correction

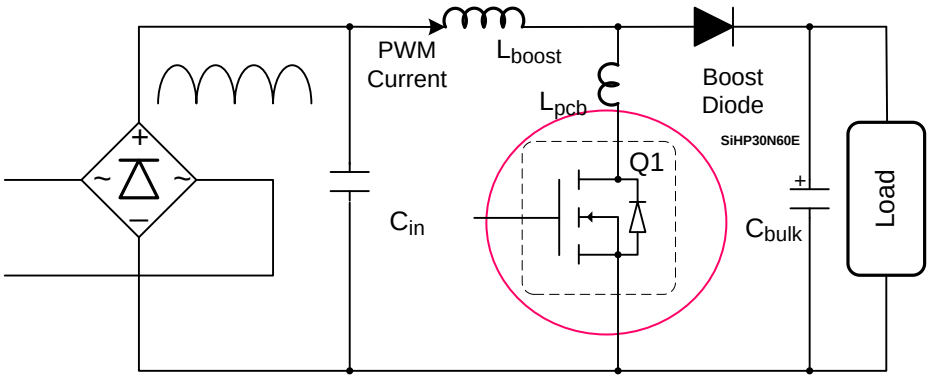


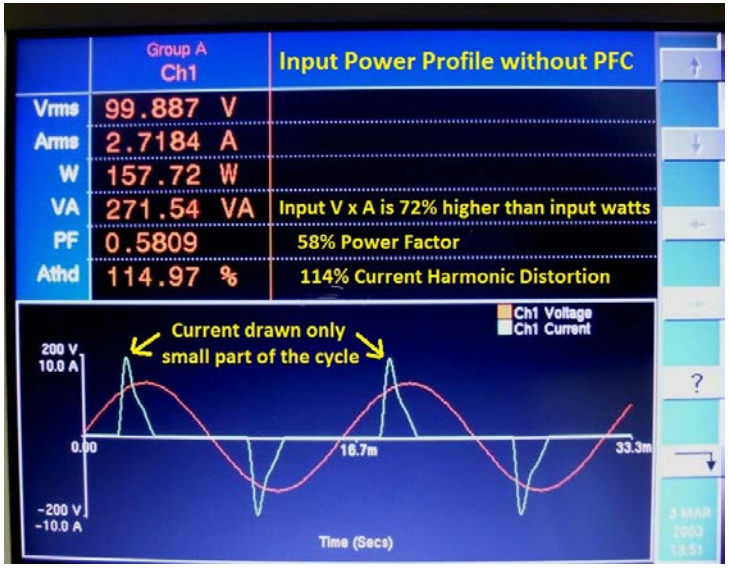
What and Why

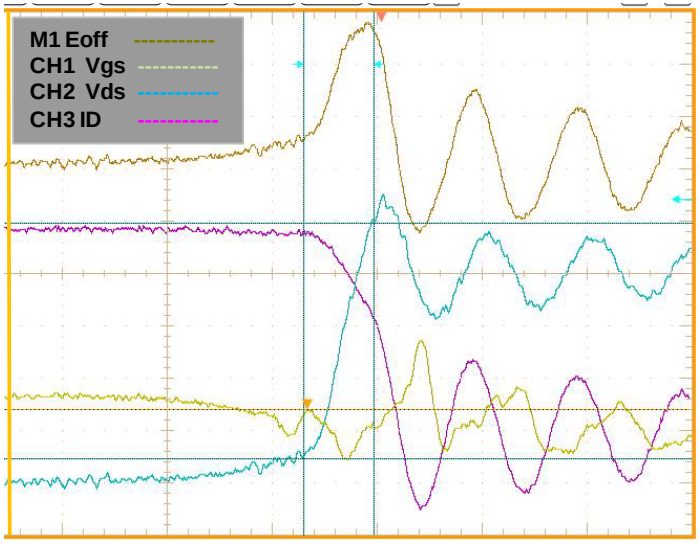
- To minimise transmission losses input current must have the same shape and phase as voltage
- Two methods for AC current shaping with voltage
- Discontinuous current method for low power
- Continuous current method for high power
- Both require input current filter to remove switching freq content

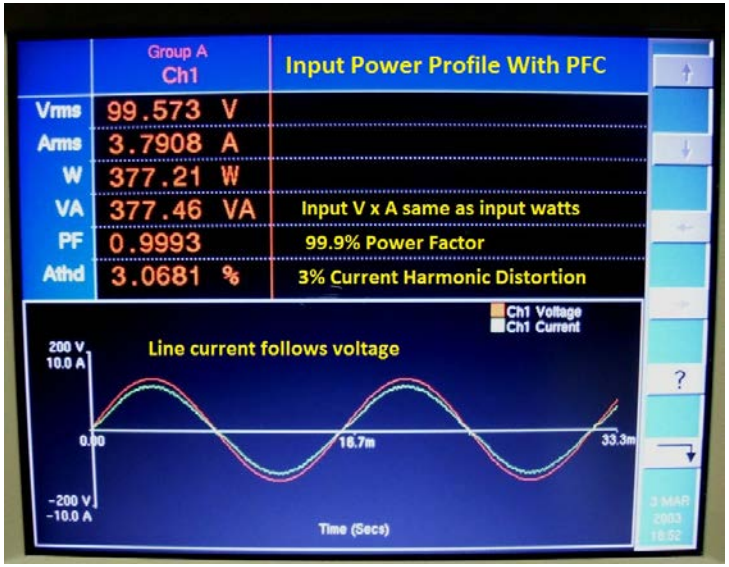
AC-DC: Power Factor Correction

- Basic PFC Operation and MOSFET Related Loss
  - 420W Platform, Vout 390V









80 Plus Certified Power Supplies

- Driving performance from standard planar technology to superjunction is the 80 Plus certification
- 80 Plus Power Supply Certification
  - The 80 Plus performance specification requires power supplies in computers and servers to be 80% or greater energy efficient at 10, 20, 50, and 100% of rated load with a true power factor of 0.9 or greater.

What is 80 PLUS certified? x

80 PLUS Certification	115V Internal Non-Redundant				230V Internal Redundant			
% of Rated Load	10%	20%	50%	100%	10%	20%	50%	100%
80 PLUS	—	80%	80%	80% / PFC .90	—			
80 PLUS Bronze	—	82%	85% / PFC .90	82%	—	81%	85% / PFC .90	81%
80 PLUS Silver	—	85%	88% / PFC .90	85%	—	85%	89% / PFC .90	85%
80 PLUS Gold	—	87%	90% / PFC .90	87%	—	88%	92% / PFC .90	88%
80 PLUS Platinum	—	90%	92% / PFC .95	89%	—	90%	94% / PFC .95	91%
80 PLUS Titanium	—	—	—	—	90%	94% / PFC .95	96%	91%

Selecting the right device for PFC

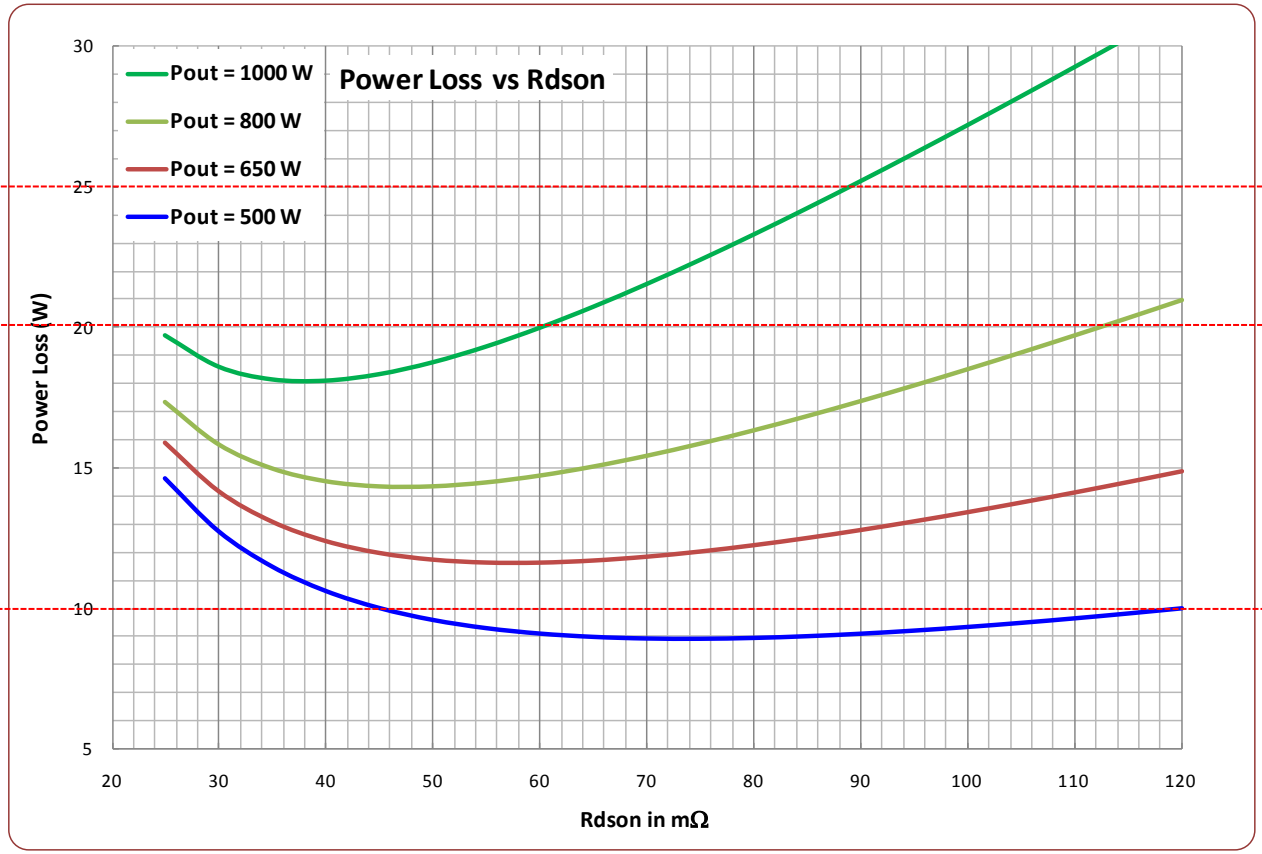
- **Full Power Loss Equations may not be immediately intuitive**
  - Often prefer simplified Figure of Merit Approach – Rds(on) * Qg
  - With the latest technology advances this may be over-simplified

$$P_{tot} = I_{ac}{}^2 \times TCR \times R_{dson} + \frac{1}{2} \times VDC \times \frac{I_{ac}}{I_{geq}} \times F_{sw} \times Q_{sw} + \frac{1}{2} \times VDC \times F_{sw} \times Q_{oss} + V_{drv} \times Q_g \times F_{sw}$$

Super TO247 Power Dissipation limit

TO247 Power Dissipation limit

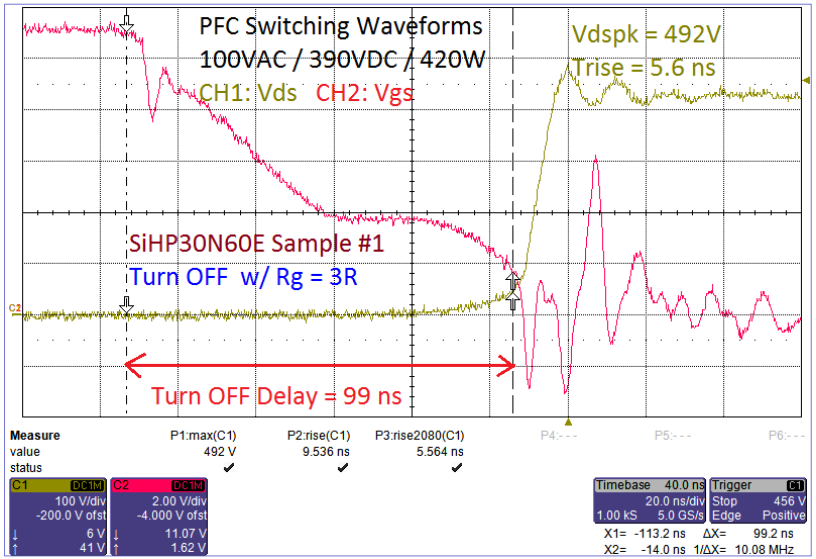
TO220 Power Dissipation limit

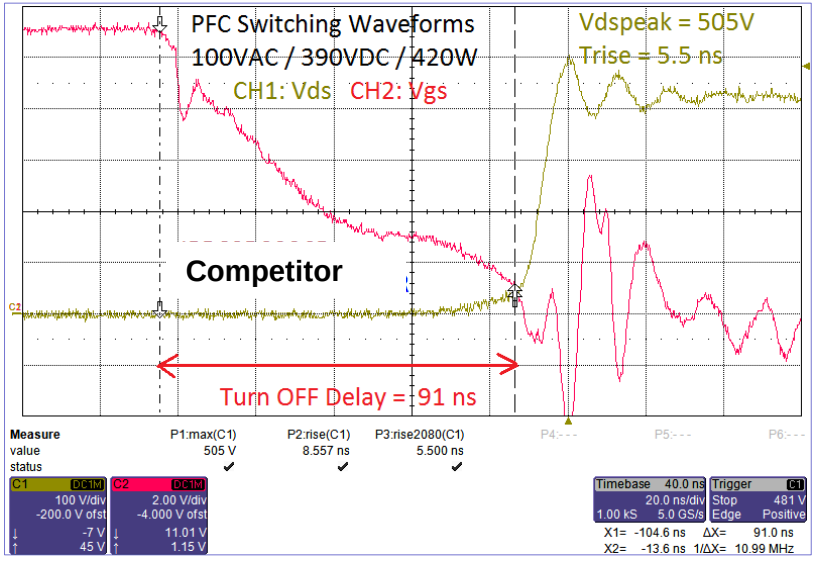


AC-DC: Power Factor Correction

- Efficiency results with fast gate drive, R_{gate} = 3 Ohm

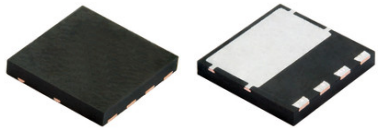
Part Number	Full Load Efficiency	Loss @ 5% Load (W)	Rds(on)	Vds peak (V)	Trise (ns)	Gate Delay (ns)
Competing device	93.09%	3.26	**90**	505	5.5	91
SiHP30N60E	93.08%	3.15	**99**	492	5.6	99
SiHP33N60E	93.09%	3.33	**82**	501	5.4	113
SiHP22N60E	92.65%	2.97	**145**			





Low Inductance Packaging – 8x8

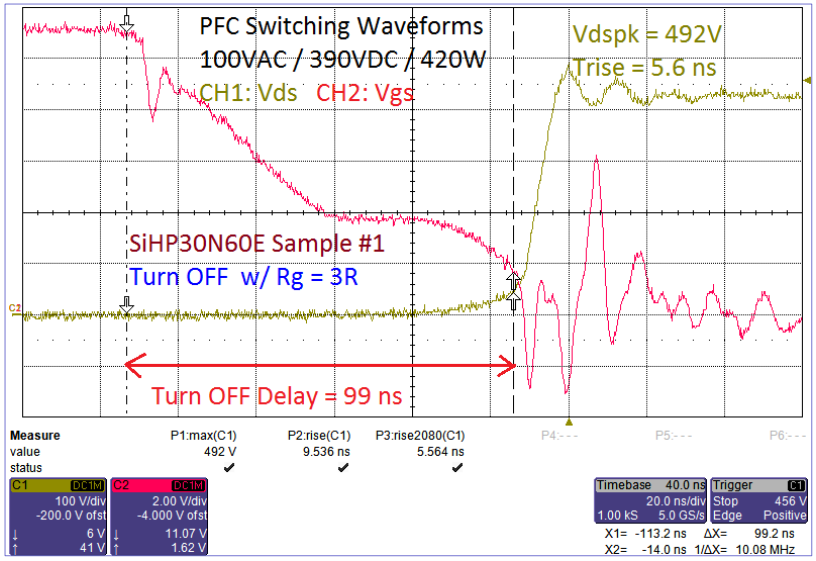
- New High Voltage MOSFET SMD
  - Small footprint 64 mm^2 with a maximum height of 1mm
  - Low inductance for fast switching HV applications
  - Kelvin source connection to reduce gate noise
  - Packaging option for high current density generations
  - Smaller than D2PAK
    - 60% footprint, 80% height, and 90% volume reduction
  - Applications
    - Server/Telecommunications
    - Adaptors
    - High power and high current density SMPS

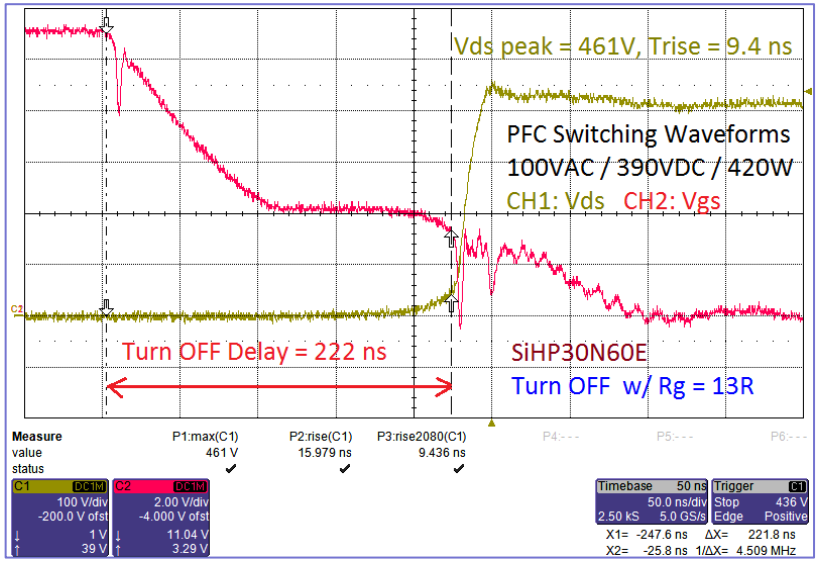


AC-DC: Power Factor Correction

- Waveform conditioning using external gate resistor
  - 13Ω vs 3Ω increases turn off delay time and rise time
  - Peak voltage reduced by 30V, but with 0.5% efficiency sacrifice

Part Number	Full Load Efficiency	Loss @ 5% Load (W)	Vds peak (V)	Trise (ns)	Gate Delay (ns)
SiHP30N60E	93.08%	3.15	492	5.6	99
SiHP30N60E High Gate Resistor	92.58%	3.16	461	9.4	222





Initial Recommendations Based on Output Power Requirement

Power Factor Correction MOSFET Selector Guide							
Pout	**Pout**	**Pout**	**Pout**	**Pout**	**Pout**	**Pout**	**Pout**
5W	**10W**	**20W**	**25W to 50W**	**75W to 100W**	**125W**	**150W**	**200W to 250W**
500V	**500V**	**500V**	**500V**	**500V**	**500V**	**500V**	**500V**
SiHx3N50D	SiHx5N50D	SiHx12N50C	SiHx12N50C	SiHx16N50C	SiHx16N50C	SiHx16N50C	SiHx18N50D
SiHx5N50D	SiHx8N50D	SiHx8N50D	SiHx8N50D	SiHx12N50C	SiHx14N50D	SiHx14N50D	SiHx16N50C
600V	**600V**	**600V**	**600V**	**600V**	**600V**	**600V**	**600V**
SIHx7N60E	SIHx7N60E	SIHx7N60E	SIHx7N60E	SiHx12N60E	SiHx12N60E	SiHx22N60E	SiHx22N60E
650V	**650V**	**650V**	**650V**	**650V**	**650V**	**650V**	**650V**
SiHx6N65E	SiHx6N65E	SiHPxN65E	SiHx6N65E	SiHx15N65E	SiHx15N65E	SiHx22N65E	SiHx22N65E

Pout	**Pout**	**Pout**	**Pout**
300W to 500W	**600 W**	**750W to 1kW**	**>1kW**
500V	**500V**	**600V**	Products Under Development
SiHS36N50D	SiHS36N50D	SiHG73N60E	
600V	**600V**	SiHG47N60E	
SiHx30N60E	SiHG33N60E	**650V**	
SiHx33N60E	SiHG47N60E	SiHG64N65E*	
650V	**650V**	SiHG47N65E	
SiHx24N65E	SiHG47N65E		
SiHx28N65E			

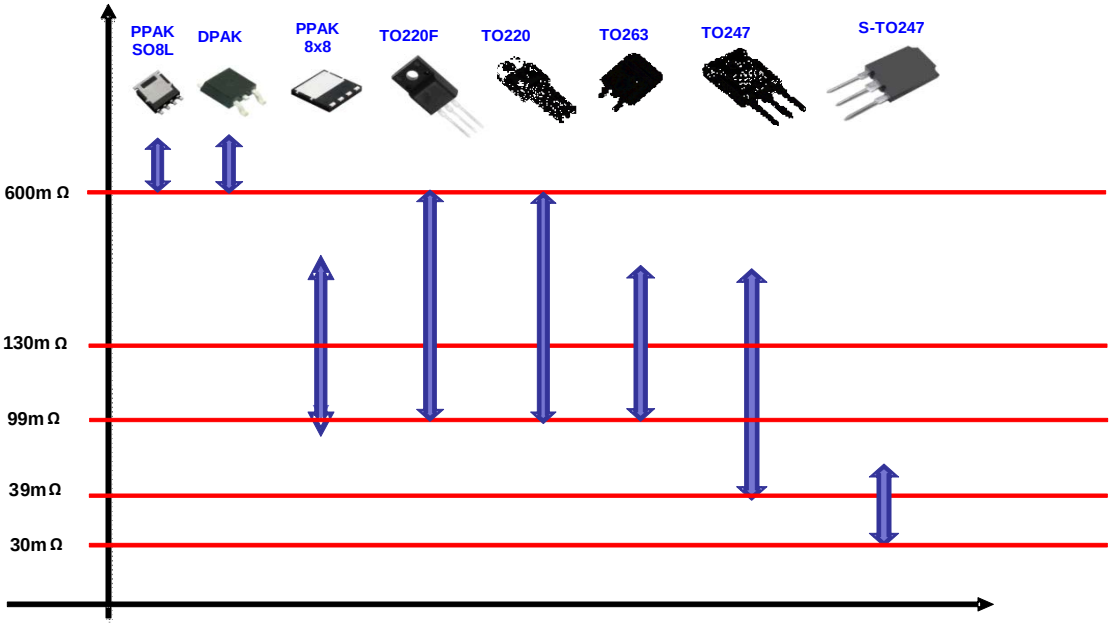
600V/650V Super Junction Technology

E Series MOSFET Technology

- **Low on-resistance:**
  - 30% reduction in on-resistance over its predecessor (S Series)
  - 39mΩ (max) to 600mΩ (max) at V_{GS} = 10V in multiple packages
  - Increased power density for new levels of efficiency with same footprint

Part Number	$V_{(BR)DSS}$ (V) (min)	I_D @ 25°C (max)	$R_{DS(ON)}$ (typ)	Q_G (nC) (typ)	C_{rss} (pF) (typ)	FOM
SiHG47N60E	600	47	0.055	146.9	5.0	8.07
Competitor 1	600	53	0.065	166.9	12.7	10.84
Competitor 2	600	47	0.058	268.8	58	13.7

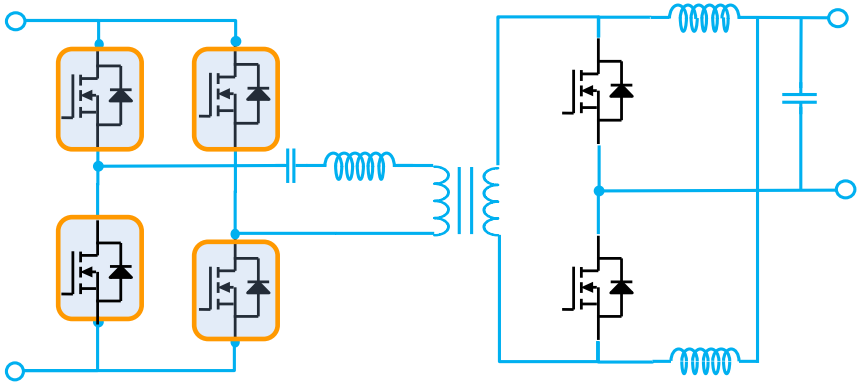
- **Provides reliable operation**
  - 100% avalanche (UIS) tested
  - High single pulse (E_{AS}) avalanche energy capability



- **Target Applications**
  - Renewable Energy (Solar Micro & Central Inverters)
  - Industrial (Welding, Battery Chargers)
  - Telecommunications (Servers, UPS)
  - Lighting (LED, HID)
  - Smart Grid (Smart Meters, Appliances)
  - General (SMPS)

Isolated DC-DC: Efficiency and FOM

Typical Isolated DC-DC Circuit Diagram



Design Focus for Isolated / ZVS DC-DC

Primary Side for Full Bridge Resonant Topology

Detail Loss Equation

$$P_d = \left(\frac{P_{th}}{V_{in}}\right)^2 \times \frac{TCR}{2} \times R_{ds} + \frac{P_{th}}{2} \times \left(\frac{Q_{sw}}{I_{gon}} + \frac{I_{ppk}}{V_{in}} \times L_{pcb}\right) \times F_{sw} + \frac{1}{4} \times V_{in} \times Q_{oss} \times F_{sw} + V_{drv} \times Q_g \times F_{sw}$$

Key Parameters for Primary Side Switch:

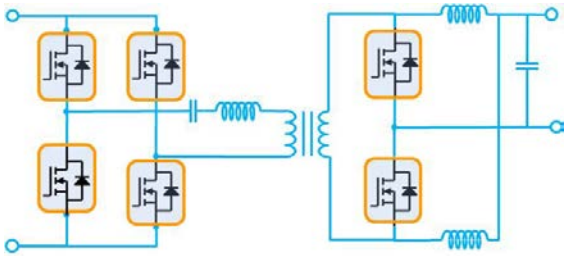
- ✓ $R_{DS(ON)}$
- ✓ Q_{Switch}
- ✓ C_{OSS} / Q_{OSS}
- ✓ Q_g

DC-DC topologies and zvs description

Various Topologies of Isolated DC-DC

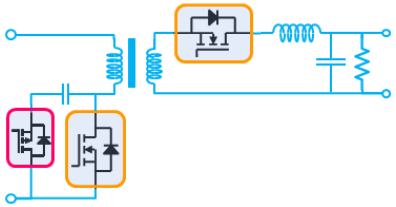
Topologies

Half/Full Bridge DC-DC Converters
Over 250W



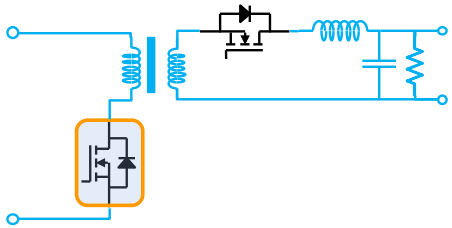
Recommended Products	Benefit to Design
SiR672DP **SiR880ADP**	Increase efficiency, power density
SiR846ADP **SiR882ADP** **SiR878ADP**	Reduce operating temperature
SiJ470DP	Reduce design size and component count
SiSS40DN	

Forward / Active Reset Forward
100W to 200W



Recommended Products	Benefit to Design
SiR872ADP	Higher efficiency, power density
	Reduce operating temperature
	Saves energy

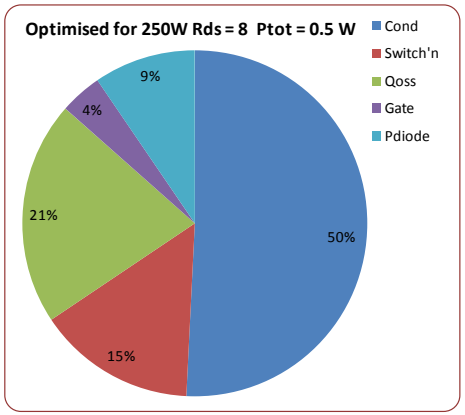
Flyback
Below 250W

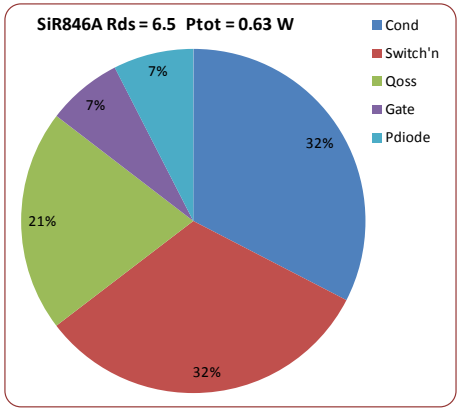


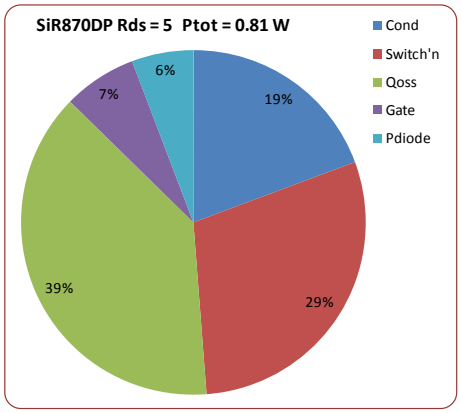
Recommended Products	Benefit to Design
SiR872ADP	Very low $R_{DS(ON)}$ Increases current output per device
	Reduce component count by minimizing devices in parallel

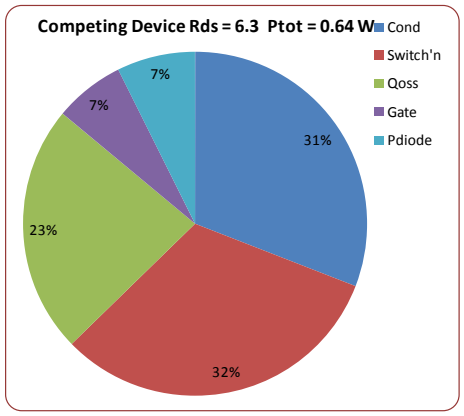
Isolated DC-DC Efficiency and Balanced Power Loss

- Balanced losses will produce the most efficient solution
  - As $R_{DS(ON)}$ is reduced in newer technology and frequencies increase, conduction losses are no longer dominant
  - Power loss from Q_{switch} and Q_{oss} contributes more than conduction loss to the total power loss









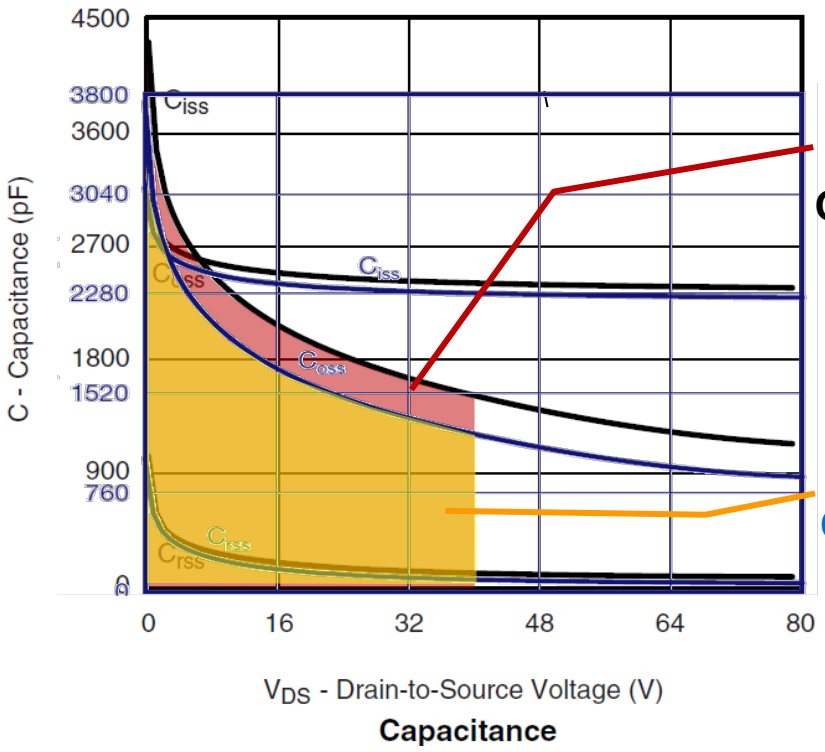
Device	R_{DS}	Q_{SW}	Q_{oss}	Q_G	Q_{rr}	V_{fwd}	Total Loss (W)
Optimized for 250W	8	4.86	43	19.4	28.0	0.75	**0.50**
Loss	**0.25**	**0.07**	**0.10**	**0.02**	**0.00**	**0.05**	
SiR846ADP	6.5	**13.3**	54	44	64	0.75	**0.63**
Loss	**0.20**	**0.20**	**0.13**	**0.04**	**0.00**	**0.05**	
SiR870DP	**5**	15.9	130	55.7	82	0.75	**0.81**
Loss	**0.16**	**0.24**	**0.31**	**0.06**	**0.00**	**0.05**	
Competing Device	6.3	13.5	62	42	112	0.75	**0.64**
Loss	**0.20**	**0.20**	**0.15**	**0.04**	**0.00**	**0.05**	

Reduce Switching Losses with Lower C_{oss} & Q_{oss}

Comparison - SiR880ADP vs. SiR880DP

Parameters	SiR880ADP	SiR880DP	Improvement
C_{oss} (pF) @ V_{DS} = 40 V	1200	1525	20%
Q_{oss} (nC)	70	85	18%

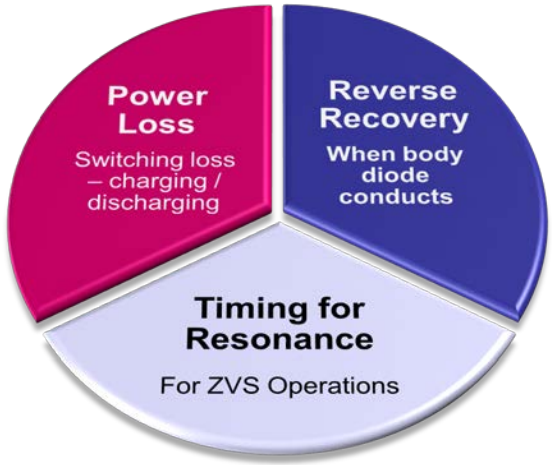
Coss Capacitance Curve



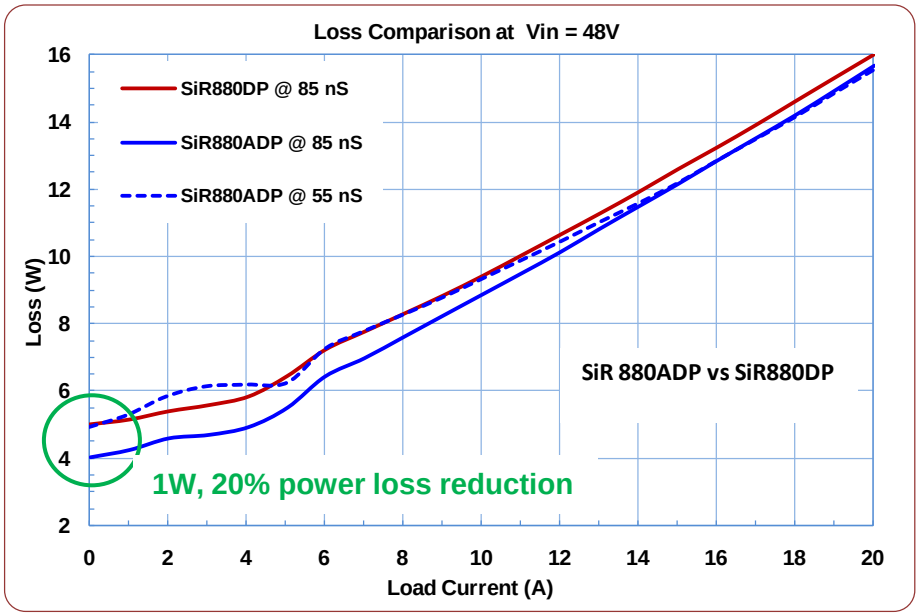
SiR880DP
Q_{oss} = 85 nC

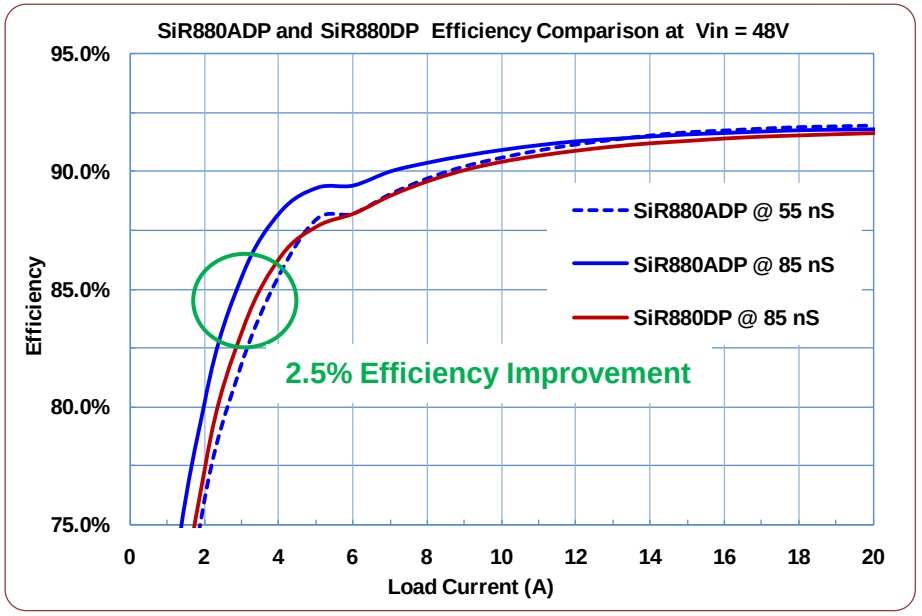
SiR880ADP
Q_{oss} = 70 nC

C_{oss} Contributes to:



C_{OSS} Reduction Improves Efficiency for ThunderFET®

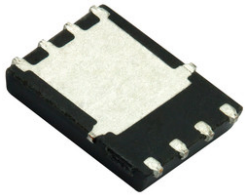




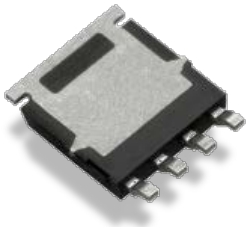
- With 20% C_{oss} reduction, SiR880ADP has uniformly lower loss compared to SiR880DP
  - At light load, the efficiency improves around 2.5%
  - 1W less power loss = 20% power loss reduction

- When dead time is reduced, ZVS is lost and the losses increase at low loads
  - At higher loads ZVS is restored and losses are almost same as longer dead time

Recommended Solution for Primary Side



PowerPAK® SO-8



PowerPAK® SO-8L
(AL Based PCB)

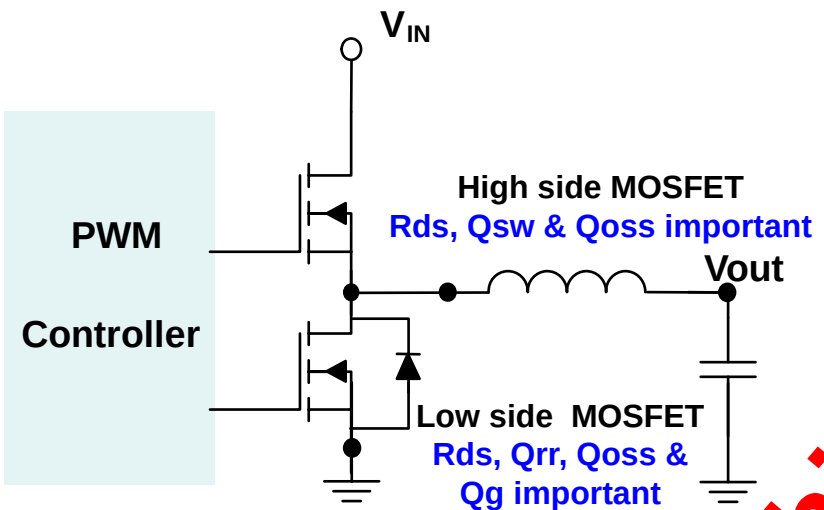
PowerPAK® 1212-8

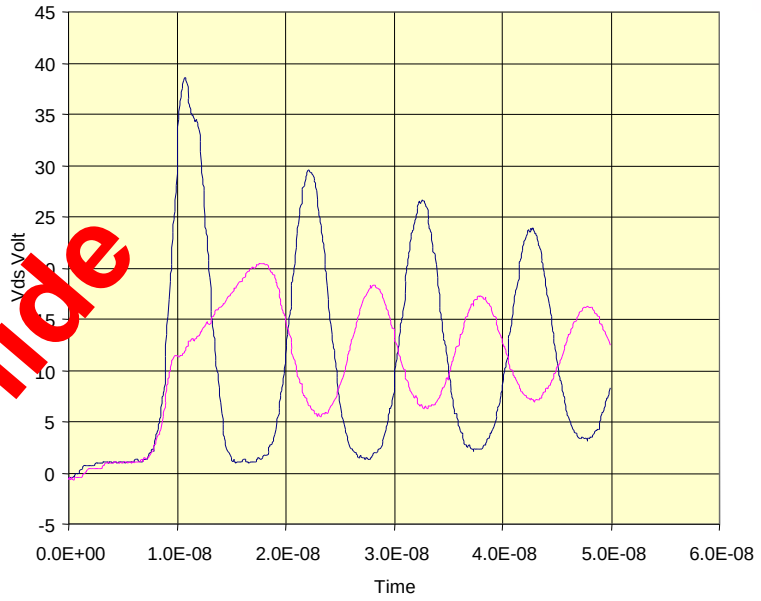
Features and Benefits:

- **Next generation 80V technology reduces $R_{DS(ON)}$ by 30% with improved dynamic specifications**
  - SiR672DP and SiS828DN
  - Increased immunity to gate coupling - Q_{GD}/Q_{GS} ratio is below 0.6
- **ThunderFET® provides low $R_{DS(ON)}$ for 5V gate drive**

Package	Part Number	V_{DS} (V)	V_{GS} (V)	$R_{DS(ON)}$ Max @10V (mΩ)	$R_{DS(ON)}$ Max @4.5V (mΩ)	Q_G Typ @10V (nC)	Q_G Typ @4.5V (nC)	Q_{GS} Typ (nC)	Q_{GD} Typ (nC)	Sample	Release
PowerPAK® SO-8	SiR672DP	80	20	4.1		57		15.3	6.9	Now	Jul 13
	SiR880ADP	80	20	5.9	8.5	49.0	23.0	8.0	12.5	Now	Now
	SiR654DP	100	20	6.9	49.5	10.8	12	1.0	811	Q3 13	Q4 13
	SiR846ADP	100	20	7.8	-	44.0	26.7	8.2	9.2	Now	Now
	SiR878ADP	100	20	14.0	18.0	27.9	13.9	4.2	6.3	Now	Now
PowerPAK® SO-8L	SiJ470DP	100	20	9.1		37	7.9	7.9	9.2	Now	Jul 13
PowerPAK® 1212	SiS828DN	80	20	13.0		16.0		3.8	2.1	Q3 13	Q4 13
	SiSS40DN	100	20	21	16	3.4	4.2	0.9	220	Now	Jul 13

DC-DC POL / VRM: Efficiency and FOM



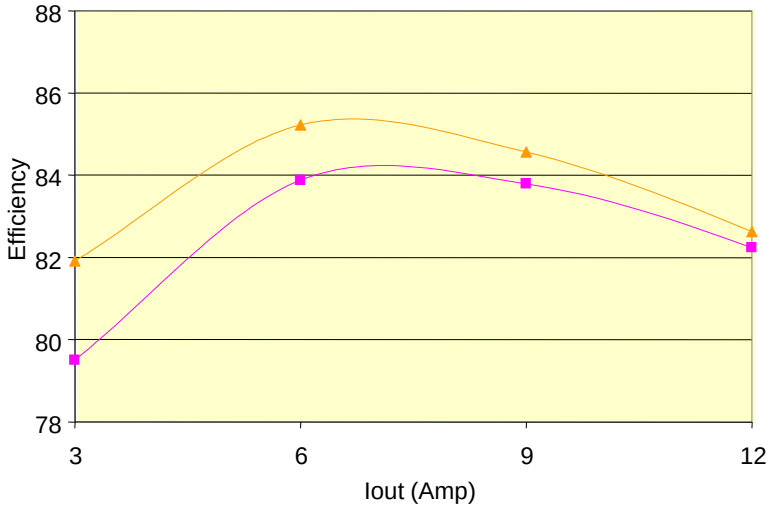


Improve this slide

Synchronous Buck: Vin = 12V. (3.3 – 20V)

Static and Dynamic Parameters important

- **Bvdss, Idss**
- **Rds(on) @ Vgs = 4.5V**
- **Qg(tot), Qgs, Qgd, Rg, Vth, Coss**
- **trr, Qrr, Vf**
- **UIS, (Peak current in avalanche)**

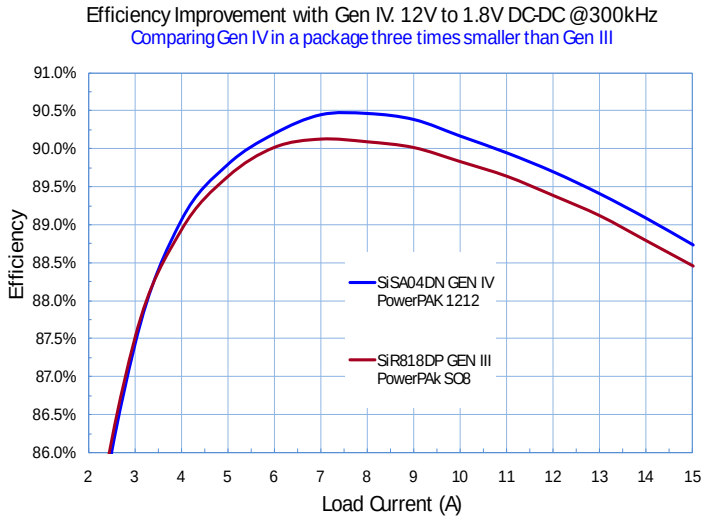


Additional FOM info

Power Density benefits realized by TrenchFET® IV

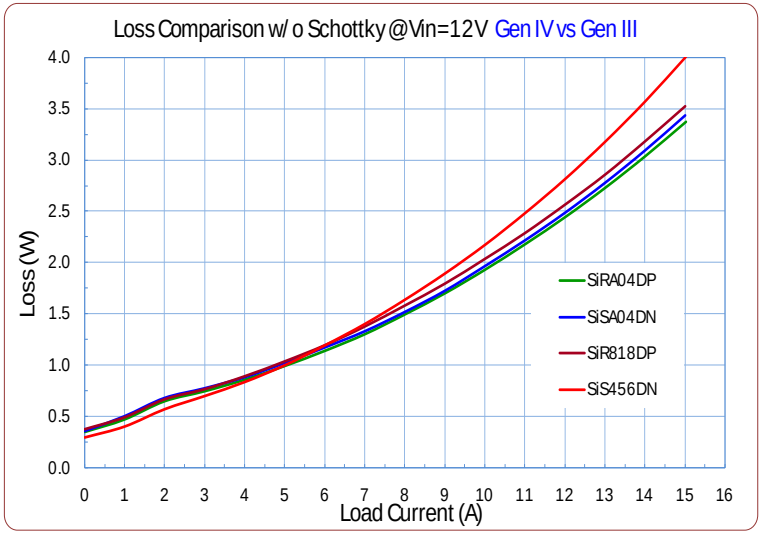
Test Condition: $12V_{IN}$ / $1.8V_{OUT}$ / 300kHZ / Up to 15A

Device	Package	Silicon	Rds(on) at 4.5V	Qg (nC)	Qgd (nc)	Qgd:Qgs	Efficiency @ 15A	P_{out} (W) / mm²
SiR818DP	PowerPAK SO-8	TrenchFET® III	2.6mΩ	30.5	9.6	1.2	88.5%	0.86
SiSA04DN	PowerPAK 1212	TrenchFET® IV	2.5mΩ	22.4	4	0.47	88.74%	2.7



SiR818DP

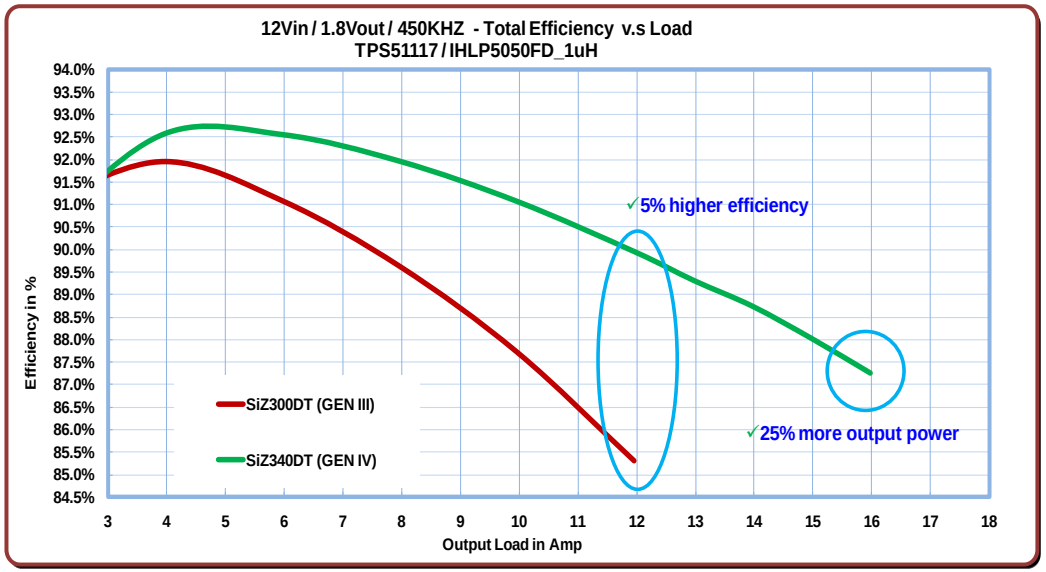
SiSA04DN

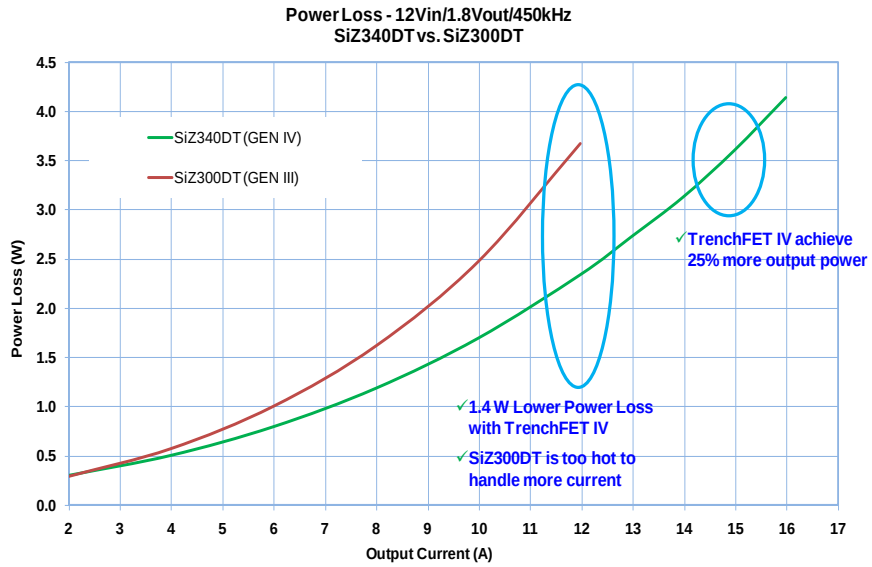


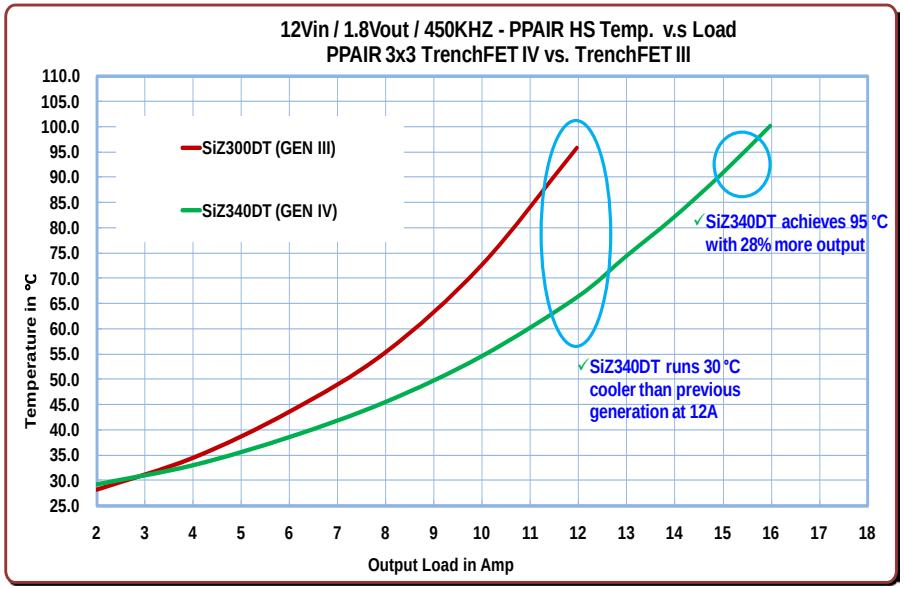
- 0.4% better peak efficiency than previous solution
- 60% smaller, lower Power Loss and temperature

Combining New Silicon with smaller integrated packages

PowerPAIR 3x3	SiZ340DT (9 mm²)		SiZ300DT (9 mm²)	
Product	HS	LS	HS	LS
Rds(on) typ. @4.5Vgs (mΩ)	11	5.5	26.5	13.5
Qg @4.5Vgs (nC)	4.8	9.7	3.5	6.8
Qgs (nC)	1.82	3.7	1.5	2.2
Qgd (nC)	0.85	1.72	1.1	2.3
Qsw (nC)	1.8	3.6	1.9	3.4
Qoss (nC)	6.6	8.3	3.3	4.4
Qrr (nC)	6	11	9	14
Vfwd (V)	0.8	0.8	0.84	0.82





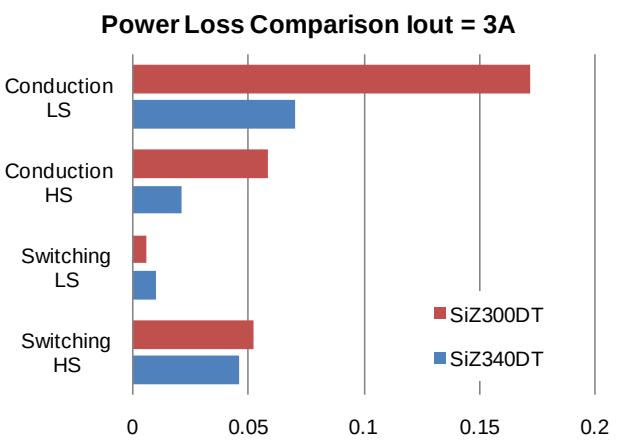


Power Loss Analysis – SiZ340DT vs. SiZ300DT

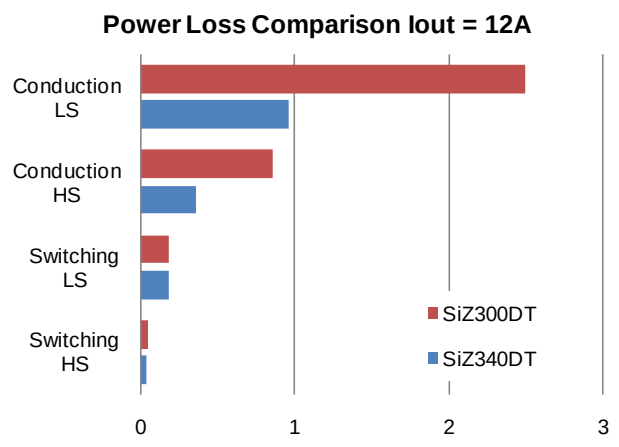
Parameter	TrenchFET IV Devices		TrenchFET III Devices	
	SiZ340DT		SiZ300DT	
	HS	LS	HS	LS
Rds(on) Typ. @ 4.5Vgs (mΩ)	11	5.5	26.5	13.5
Qg (nC)	4.8	9.7	3.5	6.8
Qsw (nC)	1.8	3.6	1.9	3.4

Contributors to Power Loss
(12Vin, 1.8Vout, 450kHz)

Iout = 3 A



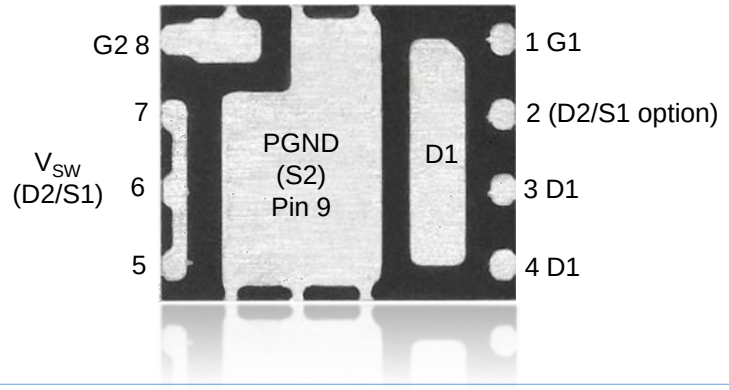
Iout = 12 A

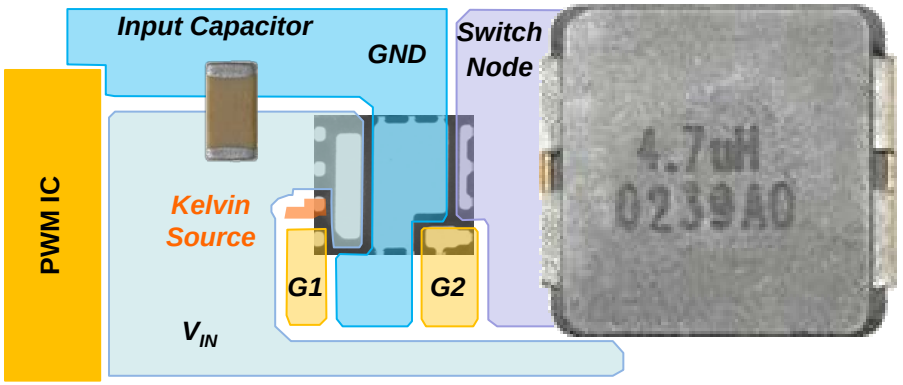


- The combination of Rds, Qg and Coss improvement allows TrenchFET IV saves more power over previous generation
  - Enables 60% low side Rds(on) reduction in PowerPAIR 3x3 package to reduce conduction loss
  - Qsw remains similar while Rds(on) is reduced
  - Qg is reduced by 50% and Qsw is reduced by 60% with similar Rds(on)

Next Generation PowerPAIR® Design

Package Bottom View	Common PCB Layout Preview



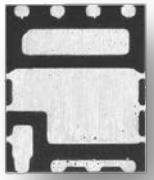


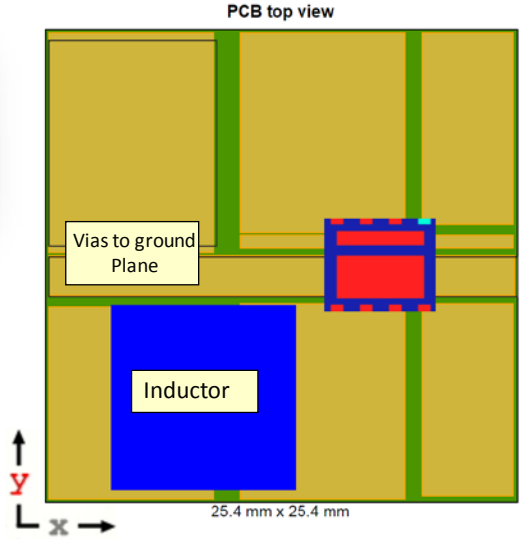
Package	Part	V_{DS} (V)	V_{GS} (V)	$R_{DS(ON)}$ 4.5V_{GS} Max (mΩ)		Q_G 4.5V (nC)		Q_{GS} (nC)		Q_{GD} (nC)		Sample	Release
				HS	LS	HS	LS	HS	LS	HS	LS		
PPAIR 6x5	SiZF904DT	30	20/-16	5	1.0	12	60	5	20	2	12	Jan 2013	Mar 2013
PPAIR 6x5	SiZF906DT	30	20/-16	5	1.5	12	45	5	17	2	9	Jan 2013	Mar 2013

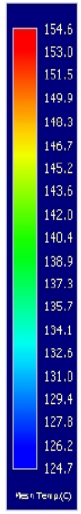
- Single-package power stage solution for 30A per phase increases power density
  - For DC-DC systems up to Vin = 20V
  - Low-side with flipped chip allows larger active area and lower $R_{DS(ON)}$
  - Kelvin Source connection improved high side switching

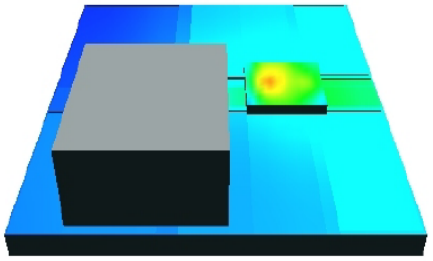
Package Design, PCB Layout and Thermal Performance

Results below obtained using ThermaSim Powered by EPSILON

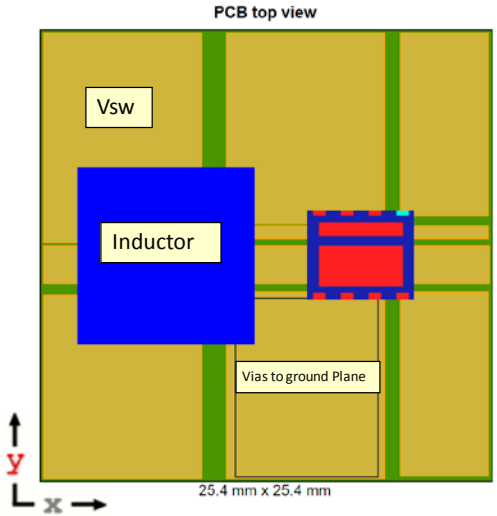


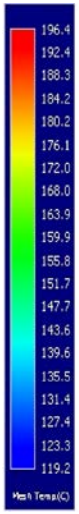


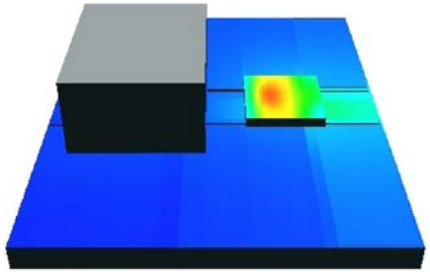




Min Device Temp	Max Device Temp	Min PCB Temp	Max PCB Temp
125ºC	155ºC	125ºC	151ºC



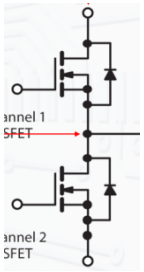


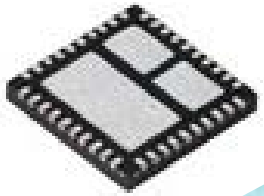


Min Device Temp	Max Device Temp	Min PCB Temp	Max PCB Temp
119ºC	196ºC	119ºC	192ºC

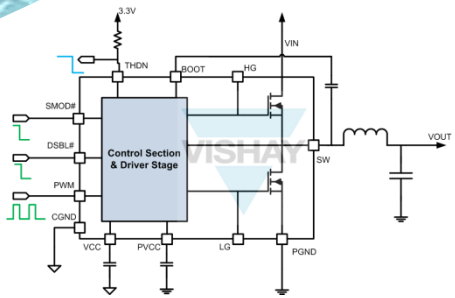
Levels of Power Stage Integration

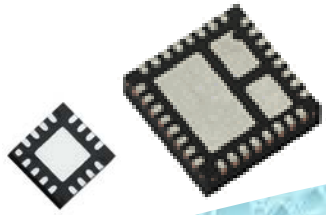
PowerPAIR®



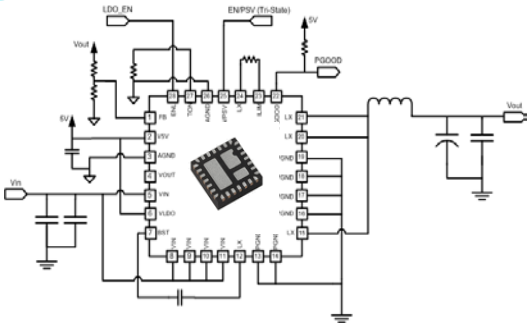


DrMOS





microBUCK™



microBRICK™

DrMOS – Integrated Power Stage

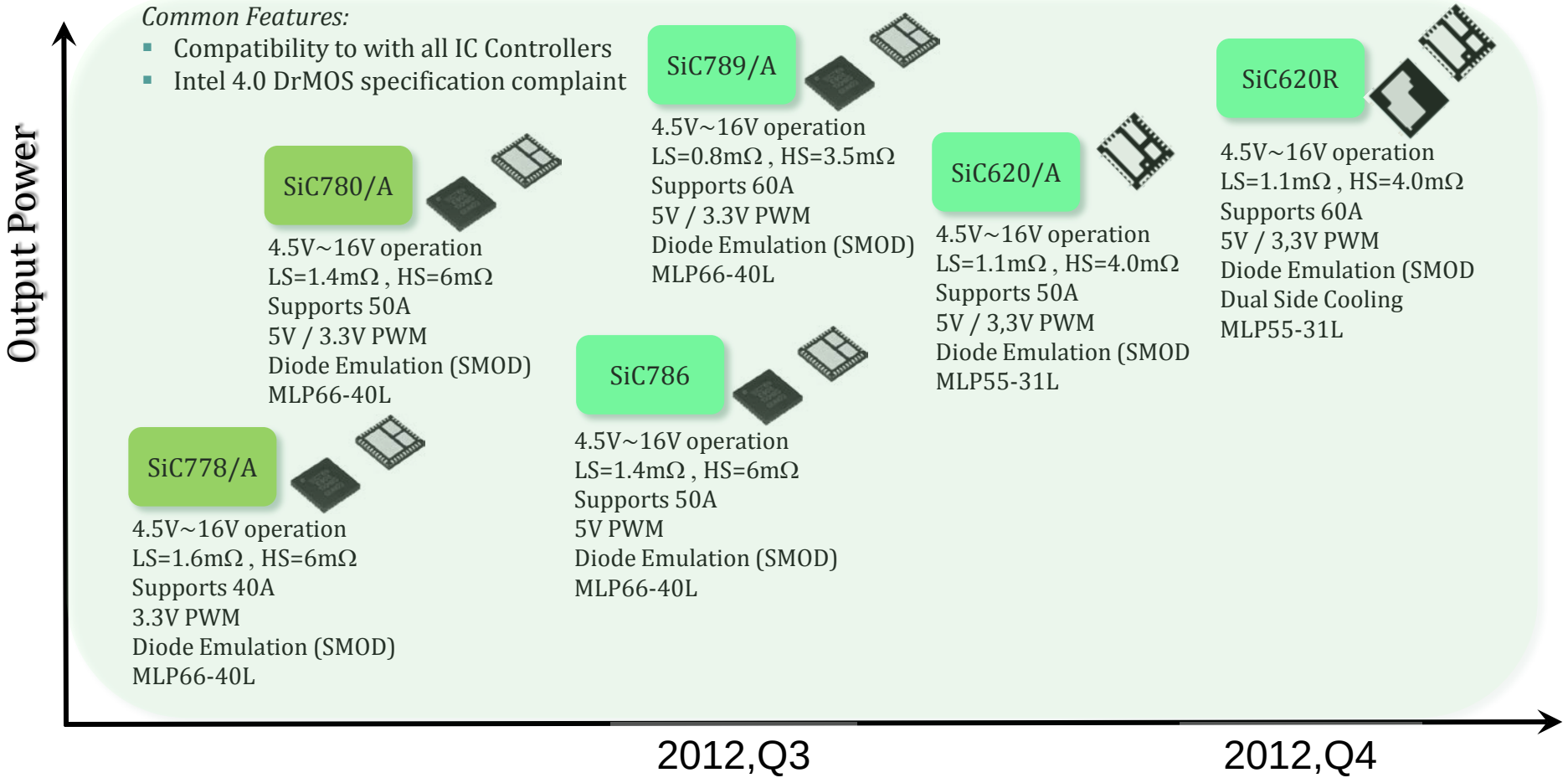
Target Applications:

Multi Phase power stage for Vcore and DDR Memory

- Server, PC, Graphic Cards

Value Proposition:

- Power Density
- High Switching Frequency
- Ease of use



microBuck® – Product Offering

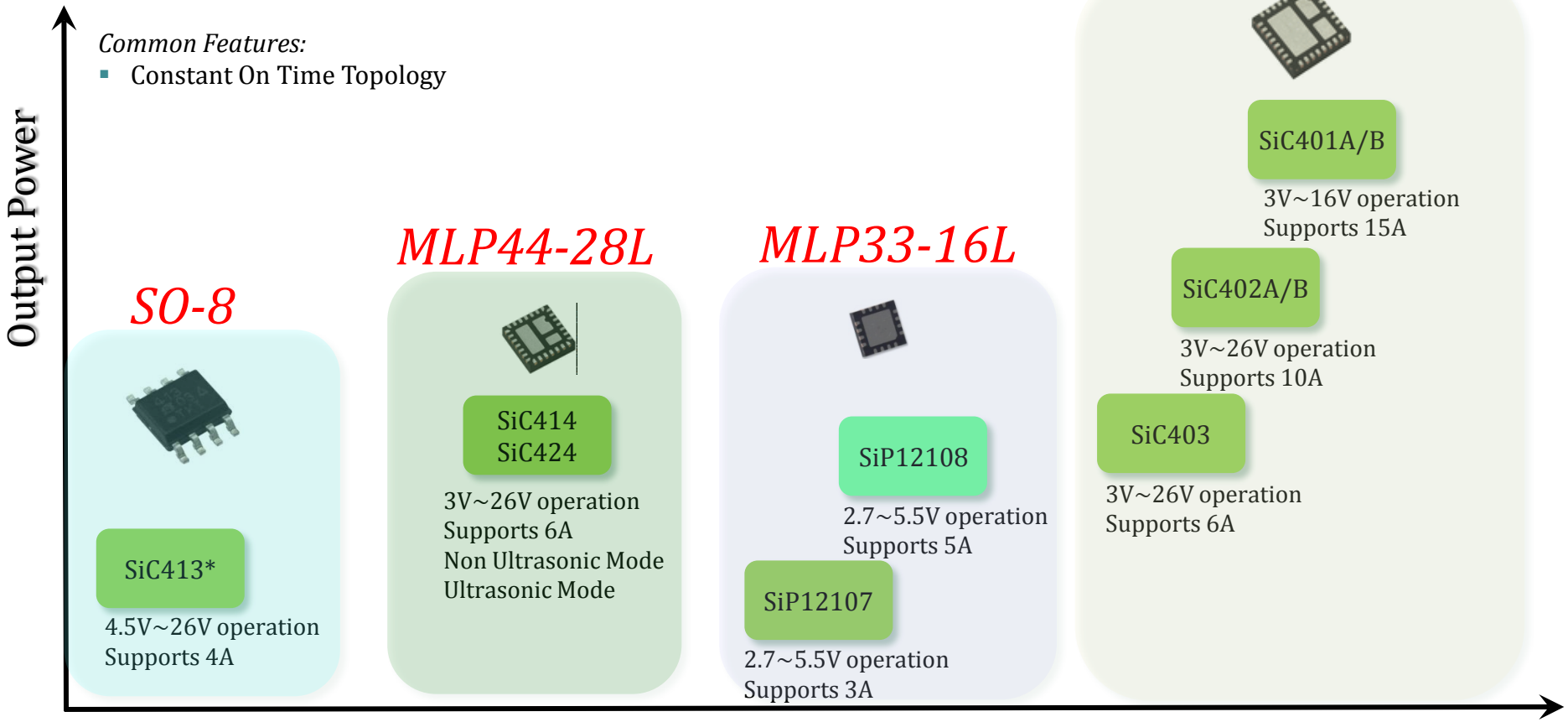
Target Applications:

Point Of Load (POL) DC\DC in

- Server, Networking, Telecom
- Notebook, Tablet

Value Proposition:

- Scalability
- All Ceramic solution
- Fast Transient
- Ease of use



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